ABSTRACT OF THE DISCLOSURE

A floating point operand testing circuit includes an analysis circuit and a result generator circuit coupled to the analysis circuit. The analysis circuit determines the status of a floating point operand based upon data within the operand. An operand buffer may supply the operand to the analysis circuit. The result generator circuit is responsive to at least one control signal and asserts a result signal if the floating point analysis circuit matches the floating point status to a predetermined format specified by the control signal. The result signal can condition the outcome of a floating point instruction. The result generator may also respond to multiple control signals asserted when testing a single operand for different formats, such as not-a-number (NaN), infinity, normalized, denormalized, invalid operation, overflow, underflow, division by zero, exact, and inexact.